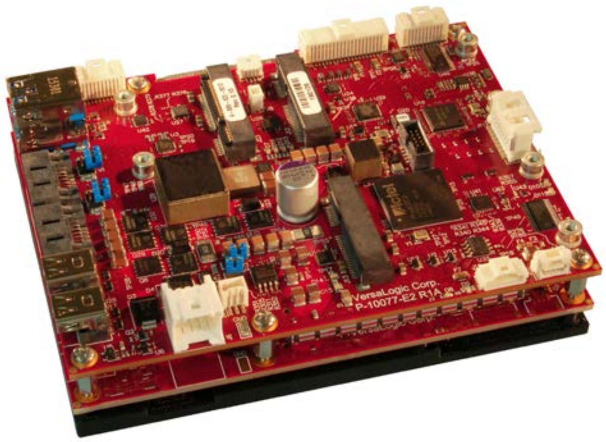

Programmer's Reference Manual

REV. May 2018

Blackbird

(VL-EPU-4562)

Intel® Core™-based Embedded Processing Unit with SATA, Dual Ethernet, USB, Digital I/O, Serial, Video, Mini PCIe Sockets, SPX, Trusted Platform Module.

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Product Release Notes

Release 1.1

Updated Uartmode1 – Uart Mode Register #1 section

Release 1.0

Initial Release.

Support

The EPU-4562 support page contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

Contents

Tables

Introduction 1

This document provides information for users requiring register-level information for developing applications with the VL-EPU-4562.

Related Documents

The following documents are available on the EPU-4562 Product Support Web Page:

- *VL-EPU-4562 Hardware Reference Manual* – provides information on the board's hardware features including connectors and all interfaces.

Operating System compatibility and software package downloads are available at the VersaLogic Software Support page.

System Resources 2

Interrupts

The LPC SERIRQ is used for interrupt interface to the Skylake SoC.

Each of the following devices can have an IRQ interrupt assigned to it and each with an interrupt enable control for IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, and IRQ11:

- 8254 timers (with three interrupt status bits)
- 8x GPIOs (with one interrupt status bit per GPIO)16x Digital I/Os (with 1 interrupt status bit per GPIO)
- COM 1 UART (with 16550 interrupt status bits)
- COM 2 UART (with 16550 interrupt status bits)
- COM 3 UART (with the usual 16550 interrupt status bits).
- COM 4 UART (with the usual 16550 interrupt status bits).
- Watchdog timer (one status bit)

Common interrupts can be assigned to multiple devices if software can deal with it (this is common on UARTs being handled by a common ISR).

Interrupt status bits for everything except the UARTs will "stick" and are cleared by a "write-one" to a status register bit. The 16550 UART interrupts behave as defined for the 16550 registers and are a pass-through to the LPC SERIRQ.

Per the VersaAPI standard, anytime an interrupt on the SERIRQ is enabled, the slot becomes active. All interrupts in the SERIRQ are high-true so when the slot becomes active, the slot will be low when there is no interrupt and high when there is an interrupt.

FPGA I/O Space

The FPGA is mapped into I/O space on the LPC bus. The address range is mapped into a 64 byte I/O window.

- FPGA access: LPC I/O space
- FPGA access size: All 8-bit byte accesses (16-bit like registers are aligned on 16-bit word boundaries to make word access possible in software but the LPC bus still splits the accesses into two 8-bit accesses)
- FPGA address range: 0x1C80 to 0x1CBF (a 64-byte window)

The three 8254 timers only require four bytes of addressing and are located at the end of the 64-byte I/O block. The only requirement is that the base address must be aligned on a 4-byte block. The table below lists the FPGA's I/O map.

Table 1: FPGA I/O Map

Address Range	Device	Size
0x1C80 – 0x1CBB	FPGA registers	60 bytes
0x1CBC – 0x1CBF	8254 timer address registers	4 bytes

FPGA Registers 3

This chapter describes the FPGA registers.

- Table 2 (beginning on the following page) lists all 64 FPGA registers
- Table 3 (refer to page 8) through Table 48 provide bit-level information on the individual FPGA registers

Register Access Key

Key:	
R/W	Read/Write
RO	Read-Only
R/WC	Read-Status/Write-1-to-Clear
WO	Write-Only
ROC	Read-Only and clear-to-0 after reading
RSVD	Not implemented. Returns 0 when read. Writes are ignored

Reset Status Key

Reset Status Key	
POR	Power-on reset (only resets one time when input power comes on)
Platform	Resets prior to the processor entering the S0 power state (that is, at power-on and in sleep states)
resetSX	• If AUX_PSEN is a '0' in MISCSR1 (default setting), then this is the same as the Platform reset. • If AUX_PSEN is programmed to a '1', then it is the same as the Power-On Reset (POR).
n/a	Reset doesn't apply to status or reserved registers

FPGA Register Map

Table 2: FPGA Register Map

I/O Address	Offset	Reset	D7	D6	D5	D4	D3	D2	D1	D0
C80	0	Platform	PLED	PRODUCT_CODE						
C81	1	n/a	REV_LEVEL					EXTEMP	CUSTOM	BETA
C82	2	Platform	BIOS_JMP	BIOS_OR	BIOS_SEL	LED_DEBUG	WORKVER	0	WP_JMP	WP_EN
C83	3	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	0	IMASK_TC5	IMASK_TC4	IMASK_TC3
C84	4	Platform	INTRTEST	TMRTEST	TMRIN4	TMRIN3	0	ISTAT_TC5	ISTAT_TC4	ISTAT_TC3
C85	5	Platform	TIM5GATE	TIM4GATE	TIM3GATE	TM45MODE	TM4CLKSEL	TM3CLKSEL	TMROCTST	TMRFULL
C86	6	n/a	0	0	0	0	0	0	0	0
C87	7	n/a	0	0	0	0	0	0	0	0
C88	8	Platform	CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0
C89	9	Platform	IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY
C8A	A	Platform	msb	<============>						lsb
C8B	B	Platform	msb	<============>						lsb
C8C	C	Platform	msb	<============>						lsb
C8D	D	Platform	msb	<============>						lsb
C8E	E	Platform	0	MUXSEL2	MUXSEL1	MUXSEL0	0	SERIRQEN	SPILB	DACLDA
C8F	F	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	ADC_RESET	IN_ALARM	ISTAT_ALARM	IMASK_ALARM
C90	10	POR	0	0	0	0	MINI3_PSDIS	MINI2_PSDIS	AUX_PSEN	MINI1_PSDIS
C91	11	POR	USB_HUBMODE	W_DISABLE	USB_HUBDIS	ETH0_OFF	USB2_OC2	USB2_OC1	USB2_DIS2	USB2_DIS1
C92	12	Platform	PROCHOT	LVDS_OC	0	0	0	PBRESET	0	TPM_PP
C93	13	POR	0	0	USB3_OC2	USB3_OC1	0	0	USB3_DIS2	USB3_DIS1
C94	14	resetSX	DIR_DIO8	DIR_DIO7	DIR_DIO6	DIR_DIO5	DIR_DIO4	DIR_DIO3	DIR_DIO2	DIR_DIO1
C95	15	resetSX	DIR_DIO16	DIR_DIO15	DIR_DIO14	DIR_DIO13	DIR_DIO12	DIR_DIO11	DIR_DIO10	DIR_DIO9
C96	16	resetSX	POL_DIO8	POL_DIO7	POL_DIO6	POL_DIO5	POL_DIO4	POL_DIO3	POL_DIO2	POL_DIO1
C97	17	resetSX	POL_DIO16	POL_DIO15	POL_DIO14	POL_DIO13	POL_DIO12	POL_DIO11	POL_DIO10	POL_DIO9
C98	18	resetSX	OUT_DIO8	OUT_DIO7	OUT_DIO6	OUT_DIO5	OUT_DIO4	OUT_DIO3	OUT_DIO2	OUT_DIO1
C99	19	resetSX	OUT_DIO16	OUT_DIO15	OUT_DIO14	OUT_DIO13	OUT_DIO12	OUT_DIO11	OUT_DIO10	OUT_DIO9
C9A	1A	n/a	IN_DIO8	IN_DIO7	IN_DIO6	IN_DIO5	IN_DIO4	IN_DIO3	IN_DIO2	IN_DIO1
C9B	1B	n/a	IN_DIO16	IN_DIO15	IN_DIO14	IN_DIO13	IN_DIO12	IN_DIO11	IN_DIO10	IN_DIO9

I/O Address	Offset	Reset	D7	D6	D5	D4	D3	D2	D1	D0
C9C	**1C**	Platform	IMASK_DIO8	IMASK_DIO7	IMASK_DIO6	IMASK_DIO5	IMASK_DIO4	IMASK_DIO3	IMASK_DIO2	IMASK_DIO1
C9D	**1D**	Platform	IMASK_DIO16	IMASK_DIO15	IMASK_DIO14	IMASK_DIO13	IMASK_DIO12	IMASK_DIO11	IMASK_DIO10	IMASK_DIO9
C9E	**1E**	Platform	ISTAT_DIO8	ISTAT_DIO7	ISTAT_DIO6	ISTAT_DIO5	ISTAT_DIO4	ISTAT_DIO3	ISTAT_DIO2	ISTAT_DIO1
C9F	**1F**	Platform	ISTAT_DIO16	ISTAT_DIO15	ISTAT_DIO14	ISTAT_DIO13	ISTAT_DIO12	ISTAT_DIO11	ISTAT_DIO10	ISTAT_DIO9
CA0	**20**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	0	0	0	TMREN
CA1	**21**	resetSX	DIR_GPIO8	DIR_GPIO7	DIR_GPIO6	DIR_GPIO5	DIR_GPIO4	DIR_GPIO3	DIR_GPIO2	DIR_GPIO1
CA2	**22**	resetSX	POL_GPIO8	POL_GPIO7	POL_GPIO6	POL_GPIO5	POL_GPIO4	POL_GPIO3	POL_GPIO2	POL_GPIO1
CA3	**23**	resetSX	OUT_GPIO8	OUT_GPIO7	OUT_GPIO6	OUT_GPIO5	OUT_GPIO4	OUT_GPIO3	OUT_GPIO2	OUT_GPIO1
CA4	**24**	n/a	IN_GPIO8	IN_GPIO7	IN_GPIO6	IN_GPIO5	IN_GPIO4	IN_GPIO3	IN_GPIO2	IN_GPIO1
CA5	**25**	Platform	IMASK_GPIO8	IMASK_GPIO7	IMASK_GPIO6	IMASK_GPIO5	IMASK_GPIO4	IMASK_GPIO3	IMASK_GPIO2	IMASK_GPIO1
CA6	**26**	Platform	ISTAT_GPIO8	ISTAT_GPIO7	ISTAT_GPIO6	ISTAT_GPIO5	ISTAT_GPIO4	ISTAT_GPIO3	ISTAT_GPIO2	ISTAT_GPIO1
CA7	**27**	resetSX	MODE_GPIO8	MODE_GPIO7	MODE_GPIO6	MODE_GPIO5	MODE_GPIO4	MODE_GPIO3	MODE_GPIO2	MODE_GPIO1
CA8	**28**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	0	RESET_EN	WDT_EN	WDT_STAT
CA9	**29**	Platform	msb	<============>						lsb
CAA	**2A**	Platform	0	0	0	0	COM4_MODE	COM3_MODE	COM2_MODE	COM1_MODE
CAB	**2B**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	0	0	0	0
CAC	**2C**	Platform	COM_MODE	0	0	0	0	0	0	FAN_OFF
CAD	**2D**	n/a	0	0	0	0	0	0	0	0
CAE	**2E**	Platform	msb	<============>						lsb
CAF	**2F**	Platform	msb	<============>						lsb
CB0	**30**	n/a	0	0	0	0	0	0	0	0
CB1	**31**	n/a	0	0	0	0	0	0	0	0
CB2	**32**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	UART1_BASE3	UART1_BASE2	UART1_BASE1	UART1_BASE0
CB3	**33**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	UART2_BASE3	UART2_BASE2	UART2_BASE1	UART2_BASE0
CB4	**34**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	UART3_BASE3	UART3_BASE2	UART3_BASE1	UART3_BASE0
CB5	**35**	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	UART4_BASE3	UART4_BASE2	UART4_BASE1	UART4_BASE0
CB6	**36**	Platform	UART4_485ADC	UART3_485ADC	UART2_485ADC	UART1_485ADC	UART4_EN	UART3_EN	UART2_EN	UART1_EN
CB7	**37**	Platform	0	0	0	0	0	0	0	FAST_MODE
CB8	**38**	n/a	0	0	0	0	0	0	0	0
CB9	**39**	n/a	0	0	0	0	0	0	0	0
CBA	**3A**	n/a	0	0	0	0	0	0	0	0

I/O Address	Offset	Reset	D7	D6	D5	D4	D3	D2	D1	D0
CBB	**3B**	n/a	0	0	0	0	0	0	0	0
CBC	**3C**	Platform	msb			<============>				lsb
CBD	**3D**	Platform	msb			<============>				lsb
CBE	**3E**	Platform	msb			<============>				lsb
CBF	**3F**	Platform	msb			<============>				lsb

FPGA Register Descriptions

Key:	
R/W	Read/Write
RO	Read-Only
R/WC	Read-Status/Write-1-to-Clear
WO	Write-Only
ROC	Read-Only and clear-to-0 after reading
RSVD	Not implemented. Returns 0 when read. Writes are ignored

PRODUCT INFORMATION REGISTERS

This register drives the PLED on the paddleboard. It also provides read access to the product code.

Table 3: PCR – Product Code and LED Register

Bit	Identifier	Access	Default	Description
7	PLED	R/W	0	Drives the programmable LED on the paddleboard. 0 – LED is off (default) 1 – LED is on
6-0	PRODUCT_CODE	RO	0010011	Product Code for the EPU-4562 (0x13)

Table 4: PSR – Product Status Register

Bit	Identifier	Access	Default	Description
7:3	REV_LEVEL[4:0]	RO	N/A	Revision level of the PLD (incremented every FPGA release) 0 – Indicates production release revision level when BETA status bit (bit 0) is set to '0' 1 – Indicates development release revision level when BETA status bit (bit 0) is set to '1'
2	EXTEMP	RO	N/A	Extended or Standard Temp Status (set via external resistor): 0 – Standard Temp 1 – Extended Temp (always set)
1	CUSTOM	RO	N/A	Custom or Standard Product Status (set in FPGA): 0 – Standard Product 1 – Custom Product or PLD/FPGA
0	BETA	RO	N/A	Beta or Production Status (set in FPGA): 1 – Beta (or Debug) 0 – Production

BIOS and Jumper Status Register

Table 5: SCR –Status/Control Register

Bit	Identifier	Access	Default	Description
7	BIOS_JMP	RO	N/A	Status of the external BIOS switch (jumper): 1 – Primary BIOS selected (the one on the COM Module) 0 – Backup BIOS selected (the one on the base board) Note: For this implementation this reads the status of the jumper all the time is essentially the “AND” of the jumper setting and (if the BIOS_OR is set to a ‘1’) the BIOS_SEL setting. Note that if BIOS_SEL sets a ‘1’ but a ‘0’ is read here then that means the external jumper is installed.
6	BIOS_OR	R/W	0	BIOS Switch (jumper) Override 0 – BIOS Select will follow the BIOS_JMP switch setting (FPGA BIOS_SEL setting has no affect) 1 – BIOS Select will follow the BIOS_SEL register setting
5	BIOS_SEL	R/W	0	BIOS Select (see BIOS_OR): 0 – Primary BIOS selected (the one on the COM Module) 1 – Backup BIOS selected (the one on the base board) Note: If the external BIOS configuration jumper is set to Backup then setting this will not have any affect. The jumper must not be installed to use this selection mode. Must have BIOS_OR set to a ‘1’ for this to have any affect.
4	LED_DEBUG	R/W	0	Debug LED (controls the yellow LED): 0 – LED is off and follows its primary function (MSATA_DAS) 1 – LED is on
3	WORKVER	RO	N/A	Status used to indicate that the FPGA is not officially released and is still in a working state. 0 – FPGA is released 1 – FPGA is in a working state (not released)
2	RESERVED	RO	N/A	Reserved. Writes are ignored; reads always return 0.
1	WP_JMP	RO	N/A	Back-up BIOS Write protect jumper status. WP_EN has to be set to a ‘0’ to read the actual jumper. 0 – Jumper is installed (write-protect is enabled) 1 – Jumper is removed (not write protected)
0	WP_EN	R/W	0	Back-up BIOS Write protect control. It drives an open-drain output. 0 – not write protected (open-drain output is Hi-Z so WP jumper can be read) 1 – write protected (drives output low)

TIMER REGISTERS

The FPGA implements an 8254-compatible timer/counter that includes three 16-bit timers.

Table 6: TICR – 8254 Timer Interrupt Control Register

Bit	Identifier	Access	Default	Description
7	IRQEN	R/W	0	8254 Timer interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	8254 Timer interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
2	IMASK_TC5	R/W	0	8254 timer #5 interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled
1	IMASK_TC4	R/W	0	8254 timer #4 interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled
0	IMASK_TC3	R/W	0	8254 timer #3 interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled

Table 7: TISR – 8254 Timer Interrupt Status Register

Bit	Identifier	Access	Default	Description
7	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
6	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
5	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
4	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
3	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
2	ISTAT_TC5	RW/C	N/A	Status for the 8254 Timer #5 output (terminal count) interrupt when read. This bit is read-status and a write-1-to-clear. 0 – Timer output (terminal count) has not transitioned from 0 to a 1 level 1 – Timer output (terminal count) has transitioned from a 0 to a 1 level
1	ISTAT_TC4	RW/C	N/A	Status for the 8254 Timer #4 output (terminal count) interrupt when read. This bit is read-status and a write-1-to-clear. 0 – Timer output (terminal count) has not transitioned from 0 to a 1 level 1 – Timer output (terminal count) has transitioned from a 0 to a 1 level
0	ISTAT_TC3	RW/C	N/A	Status for the 8254 Timer #3 output (terminal count) interrupt when read. This bit is read-status and a write-1-to-clear. 0 – Timer output (terminal count) has not transitioned from 0 to a 1 level 1 – Timer output (terminal count) has transitioned from a 0 to a 1 level

Table 8: TCR – 8254 Timer Control Register

Bit	Identifier	Access	Default	Description
7	TMR5GATE	R/W	0	Debug/Test Only: Controls the "gate" signal on 8254 timer #5 when not using an external gate signal: 0 – Gate on signal GCTC5 is disabled 1 – Gate on signal GCTC5 is enabled Always set to 0 when configuring timer modes except when TMRFULL is '0' and then it should be set to '1' and not changed unless using internal clocking.
6	TMR4GATE	R/W	0	Debug/Test Only: Controls the "gate" signal on 8254 timer #4 when not using an external gate signal: 0 – Gate on signal GCTC4 is disabled 1 – Gate on signal GCTC4 is enabled Always set to 0 when configuring timer modes except when TMRFULL is '0' and then it should be set to '1' and not changed unless using internal clocking
5	TMR3GATE	R/W	0	Debug/Test Only: Controls the "gate" signal on 8254 timer #3 when not using an external gate signal: 0 – Gate on signal GCTC3 is disabled 1 – Gate on signal GCTC3 is enabled Always set to 0 when configuring timer modes except when TMRFULL is '0' and then it should be set to '1' and not changed unless using internal clocking
4	TM45MODE	R/W	0	Mode to set timers #4 and #5 in: 0 – Timer #4 and #5 form one 32-bit timer controlled by timer #1 signals 1 – Timer #4 and Timer #5 are separate 16-bit timers with their own control signals. Almost always used in 32-bit mode especially when TMRFULL is a '0' (the 16-bit timer #5 if of limited use)
3	TM4CLKSEL	R/W	0	Timer #4 Clock Select: 0 – Use internal 4.125 MHz clock (derived from LPC clock) 1 – Use external ICTC4 assigned to digital I/O Timer #5 is always on internal clock if configured as a 16-bit clock
2	TM3CLKSEL	R/W	0	Timer #3 Clock Select: 0 – Use internal 4.125 MHz clock (derived from LPC clock) 1 – Use external ICTC3 assigned to digital I/O
1	TMROCTST	R/W	0	Debug/Test Only: Used to derive OCTCx outputs with TIMxGATE signals for continuity testing only: 0 – Normal operation 1 – Drive OCTCx outputs with corresponding TMRxGATE control registers (for example, OCTC4 with TMR4GATE) for continuity testing.
0	TMRFULL	R/W	0	This bit can be read or written to, but it has no function.

Miscellaneous FPGA Registers

MISCSR1 – Miscellaneous Control Register #1

This is a register in the always-on power well of the FPGA. It holds its state during sleep modes and can only be reset by a power cycle. This is a placeholder register for features like pushing the power-button and also for software initiated resets should those be needed.

Reset: This register is only reset by the main power-on reset since it must maintain its state in Sleep modes (for example, S3).

Table 9: MISCSR1 – Misc. Control Register #1

Bits	Identifier	Access	Default	Description
7-4	Reserved	RO	00000	Reserved. Writes are ignored; reads always return 0.
2	MINI2_PSDIS	R/W	0	Minicard #2 3.3 V power disable 0 – Minicard 3.3 V power stays on always (this is normally how minicards operate if they support any Wake events) 1 – Minicard 3.3 V power will be turned off when not in S0 (in sleep modes). The Minicard 3.3 V power switch is controlled by the "OR" of the S0 power control signal and the inverse of MINI2_PSDIS.
1	AUX_PSEN	R/W	0	CBR-4005B 8xGPIO (sometimes called "AUX" GPIOs) I/O Power Enable 0 – The GPIO pullups will be powered down in sleep modes (only power in S0) 1 – The GPIO pullups will not be powered down in sleep modes and the configuration will remain. This power is used for both the GPIO pullup voltage and for the 3.3V power on Pin 37 of the User Interface connector J2. **Note:** Some register resets are conditional on the state of AUX_PSEN
0	MINI1_PSDIS	R/W	0	Minicard #1 3.3 V power disable 0 – Minicard 3.3 V power stays on always (this is normally how minicards operate if they support any Wake events) 1 – Minicard 3.3 V power will be turned off when not in S0 (in sleep modes). The Minicard 3.3 V power switch is controlled by the "OR" of the S0 power control signal and the inverse of MINI1_PSDIS.

MISCSR2 – Miscellaneous Control Register #2

This is a register in the always-on power well of the FPGA. It holds its state during sleep modes and can only be reset by a power cycle. It is primarily used for control signals for the always-powered Ethernet controllers and the USB hubs. This register is only reset by the main power-on reset since it must maintain its state in sleep modes (for example, S3).

Table 10: MISCSR2 – Misc. Control Register #2

Bit	Identifier	Access	Default	Description
7	USB_HUBMODE	R/W	0	Determines whether the hub resets only once (to support wake-up from sleep modes on USB ports) or resets every time it enters sleep modes using the platform reset: 0 – USB Hub will be reset once at power on. Use USB_HUBDIS to manually control the reset if necessary. This supports USB Wake-up modes 1 – USB Hub will be reset by platform reset every time (will be reset when entering all sleep modes). USB ports cannot be used to wake-up
6	W_DISABLE	R/W	0	Controls the W_DISABLE (Wireless Disable) signal going to the PCIe Minicards (disables both minicards if asserted): 0 – W_DISABLE signal is not asserted (Enabled) 1 – W_DISABLE signal is asserted (Disabled) **Note:** There are other control sources that can be configured to control this signal and if enabled the control becomes the "OR" of all sources
5	USB_HUBDIS	R/W	0	Control the reset on the USB2513B Hub (used for 3x Minicard USB ports). 0 – USB2513 Hub is Enabled (reset released) 1 – USB2513 Hub is in Reset **Note:** FPGA was changed so that Platform reset drives this reset once at power on.
4	ETHOFF0	R/W	0	Disables Ethernet controller #0 (controls the ETH_OFF# input to the I210-IT): 0 – Ethernet controller is enabled (On) 1 – Ethernet controller is disabled (Off)
3	USB2_OC2	RO	N/A	Overcurrent Status from the USB 2.0 port 2,3 VBUS power switches. This signal also passed to the fourth USB_6_7_OC# input on the COM Express connector. 0 – VBUS power switch is not in overcurrent (either OK or disabled) 1 – VBUS power switch is in overcurrent and is now off. **Note:** The power switches latch-off in overcurrent and can only be re-enabled by a power-cycle or by setting this bit to a '1', wait >1msec and then a '0'
2	USB2_OC1	RO	N/A	Overcurrent Status from the USB 2.0 port 0,1 VBUS power switches. This signal also passed to the third USB_4_5_OC# input on the COM Express connector. 0 – VBUS power switch is not in overcurrent (either OK or disabled) 1 – VBUS power switch is in overcurrent and is now off. **Note:** The power switches latch-off in overcurrent and can only be re-enabled by a power-cycle or by setting this bit to a '1', wait >1msec and then a '0'
1	USB2_DIS2	R/W	0	Disable control for the paddleboard USB 2.0 ports 2,3 VBUS power switches (there are two power-switches but they have a common power enable and overcurrent status) 0 – VBUS power switches are enabled 1 – VBUS power switched are disabled. **Note:** The power switches latch-off in overcurrent and can only be re-enabled by a power-cycle or by setting this bit to a '1', wait >1msec and then a '0'

Bit	Identifier	Access	Default	Description
0	USB2_DIS1	R/W	0	Disable control for the paddleboard USB 2.0 ports 0,1 VBUS power switches (there are two power-switches but they have a common power enable and overcurrent status) 0 – VBUS power switches are enabled 1 – VBUS power switched are disabled. **Note:** The power switches latch-off in overcurrent and can only be re-enabled by a power-cycle or by setting this bit to a '1', wait >1msec and then a '0'

MISCSR3 – Miscellaneous Control Register #3

This register enables software to "push" the reset button.

Table 11: MISCSR3 – Misc. Control Register #3

Bits	Identifier	Access	Default	Description
7	PROCHOT	RO	N/A	The status of the THERMTRIP signal from the CPU module. 0 – THERMTRIP is not asserted (not hot) 1 – THERMTRIP is asserted
6	LVDS_OC	RO	N/A	The overcurrent status from the LVDS panel power switch. If this is ever asserted, the LVDS panel enable signal must be de-asserted and then asserted to "unlatch" the power fault condition on the power switch. 0 – LVDS Overcurrent is not asserted 1 – LVDS Overcurrent is asserted
3-5	Reserved	RO	N/A	Reads the overcurrent status for the USB paddleboard power switches (there are two power switches for the four ports but they have a common overcurrent status). 0 – Overcurrent is not asserted (power switch is on) 1 – Overcurrent is asserted (power switch is off)
2	PBRESET	R/W	---	When written to, this will do the same thing as pushing the reset button, which could be useful for a software-initiated watchdog. 0 – No action 1 – Activate the reset push-button **Note:** Because this generates a reset that will reset this register, it isn't likely a value of a '1' can ever be read-back, so it is somewhat "write-only".
1-0	Reserved	RO	00	Reserved. Writes are ignored; reads always return 0.

MISCSR4 – Miscellaneous Control Register #4

This register is used to monitor the overcurrent status of the 2x USB 3.0 VBUS power switch.

Table 12: MISCSR4 – Misc. Control Register #4

Bits	Identifier	Access	Default	Description
7	RESERVED	RO	0	Reserved – Writes are ignored. Reads always return 0
6	RESERVED	RO	0	Reserved – Writes are ignored. Reads always return 0
5	USB3_OC2	RO	N/A	The status of the overcurrent signal on VBUS power switch for second USB 3.0 Port 2. This signal also passed to the second USB_2_3_OC# input on the COM Express connector. 0 – USB 3.0 VBUS power switch is operating normally or it is disabled 1 – USB 3.0 VBUS power switch is in an overcurrent shutdown state and must be restarted
4	USB3_OC1	RO	N/A	The status of the overcurrent signal on VBUS power switch for first USB 3.0 Port 1. This signal also passed to the first USB_0_1_OC# input on the COM Express connector. 0 – USB 3.0 VBUS power switch is operating normally or it is disabled 1 – USB 3.0 VBUS power switch is in an overcurrent shutdown state and must be restarted
3	RESERVED	RO	0	Reserved – Writes are ignored. Reads always return 0
2	RESERVED	RO	0	Reserved – Writes are ignored. Reads always return 0
1	USB3_DIS2	R/W	0	Used to control the enable on VBUS power switch for second USB 3.0 Port 2. 0 – USB 3.0 VBUS power switch is enabled 1 – USB 3.0 VBUS power switch is disabled
0	USB3_DIS1	R/W	0	Used to control the enable on VBUS power switch for first USB 3.0 Port 1. 0 – USB 3.0 VBUS power switch is enabled 1 – USB 3.0 VBUS power switch is disabled

SPI CONTROL REGISTERS

These are placed at the traditional offset 0x8 location. Only external SPX interface devices use this interface. Because the board uses a 9-pin SPX connector, only two devices are supported.

SPICONTROL

Table 13: SPI Interface Control Register

Bit	Identifier	Access	Default	Description
7	CPOL	R/W	0	SPI clock polarity – Sets the SCLK idle state. 0 – SCLK idles low 1 – SCLK idles high
6	CPHA	R/W	0	SPI clock phase – Sets the SCLK edge on which valid data will be read. 0 – Data is read on rising edge 1 – Data is read on falling edge
5-4	SPILEN(1:0)	R/W	00	Determines the SPI frame length. This selection works in manual and auto slave select modes. 00 – 8-bit 01 – 16-bit 10 – 24-bit 11 – 32-bit
3	MAN_SS	R/W	0	Determines whether the slave select lines are asserted through the user software or are automatically asserted by a write to SPIDATA3. 0 - The slave select operates automatically 1 - The slave select line is controlled manually through SPICONTROL bits SS[2:0]
2-0	SS(2:0)	R/W	000	SPI slave device selection: 000 – None 001 – SS0# 010 – SS1# 011 – Undefined (ignored) 100 – Undefined (ignored) 101 – Undefined (ignored) 110 – Undefined (ignored) 111 – Undefined (ignored)

SPISTATUS

The SPX interrupt is not connected on this product. The control bits and status associated are still defined in the register set but the SPX interrupt will always be de-asserted.

Table 14: SPI Interface Status Register

Bits	Identifier	Access	Default	Description
7-6	IRQSEL[1:0]	R/W	00	The SPX interrupt is not connected on this product (always de-asserted). Selects which IRQ will be enabled if HW_IRQ_EN = 1. Interrupts are not used on this board, so this just becomes a read/write non-functional field. 00 – IRQ3 01 – IRQ4 10 – IRQ5 11 – IRQ10 **Note:** These are the first four interrupts in the “usual” LPC SERIRQ group of eight interrupts.
5-4	SPICLK(1:0)	R/W	00	Selects one of four SCLK frequencies. This is based on a 33 MHz LPC clock. 00 – 0.75Mhz(24Mhz/32) 01 – 1.5 Mhz(24Mhz/16) 10 – 2 Mhz(24 Mhz/8) 11 – 6 Mhz (24Mhz/4)
3	HW_IRQ_EN	R/W	0	The SPX interrupt is not connected on this product (always de-asserted). This enables the selected IRQ to be activated by a SPI device that is configured to use its interrupt capability. 0 - IRQs are disabled for SPI operations. 1 - The IRQ can be asserted
2	LSBIT_1ST	R/W	0	Controls the SPI shift direction from the SPIDATA(x) registers. 0 - Data is left-shifted (MSB first). 1 - Data is right-shifted (LSB first)
1	HW_INT	RO	0	SPX interrupt is not connected on this product (always de-asserted). Status flag which indicates when the hardware SPX signal SINT# is asserted. 0 - The hardware interrupt SINT# is de-asserted. 1 - An interrupt is present on SINT# If HW_IRQ_EN= 1, the selected IRQ will also be asserted by the hardware interrupt. HW_INT is read-only and is cleared when the external hardware interrupt is no longer present.
0	BUSY	RO	N/A	Status flag which indicates when an SPI transaction is underway. I^2C is so slow that there is no reason to ever poll this. 0 - The SPI bus is idle. 1 - SCLK is clocking data in/out of the SPIDATA(x) registers (that is, busy)

SPI DATA REGISTERS

There are four data registers used on the SPI interface. How many are used depends on the device being communicated with. SPIDATA0 is typically the least significant byte and SPIDATA3 is the most significant byte. Any write to the most significant byte SPIDATA3 initiates the SCLK and, depending on the MAN_SS state, will assert a slave select to begin an SPI bus transaction.

Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first and received data will be shifted in the LSbit of the selected frame size determined by SPILEN1 and SPILEN0. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first and the received data will be shifted in the MSbit of SPIDATA3.

SPIDATA0 (Least Significant Byte)

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPIDATA1

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPIDATA2

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPIDATA3 (Most Significant Byte) [Cycle Trigger Register]

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPI DEBUG CONTROL REGISTER AND MSATA/PCIE SELECT CONTROL REGISTER

This register is only used to set an SPI loopback (debug/test only) but is also used for the mSATA/PCIe Minicard Mux select.

Table 15: SPI – SPI Debug Control Register

Bit	Identifier	Access	Default	Description
7	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
6-4	MUXSEL(2:0)	R/W	000	mSATA/PCIe Mux selection for Minicard slot (and 2nd SATA connector): • 000 – Select mSATA using only pin 43 (MSATA_DETECT). This is an Intel-mode that is reliable for PCIe Minicards but not for mSATA modules that inadvertently ground this signal. • 001 – Use only Pin 51 (PRES_DISABLE2#). This is the default method and is defined in the Draft mSATA spec but some Minicards use it as a second wireless disable. • 010 – Use either Pin 43 or Pin 51. This will work just like 001 because Pin 43 is disabled by an FPGA pull-down. • 011 – Force PCIe mode on the Minicard • 100 – Force mSATA mode on the Minicard. • 101 – Undefined (same as 000) • 110 – Undefined (same as 000) • 111 – Undefined (same as 000) **Note:** When the Minicard uses PCIe, the SATA channel automatically switches to the SATA connector.
3	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
2	SERIRQEN	R/W	0	When an IRQ is assigned a slot in the SERIRQ, it will drive the slot with the interrupt state, but this bit must be set to a '1' to do that. 0 – Slots assigned to SERIRQ are not driven (available for other devices). 1 – Slots assigned to SERIRQ are driven with their current interrupt state (which is low since interrupts are high-true). This is because the default interrupt settings in this FPGA can conflict with other interrupts if the VersaAPI is not being used (for example, console redirect using IRQ3).
1	SPILB	R/W	0	Debug/Test Only: Used to loop SPI output data back to the input (debug/test mode). 0 – Normal operation 1 – Loop SPI output data back to the SPI input data (data output still active)
0	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.

ADM – ADC CONTROL/STATUS REGISTER

This register is used as the interrupt control/status register for the TI ADS8668A and is primarily related to the ALARM signal output from the A/D**.**

Bit	Identifier	Access	Default	Description
7	IRQEN	R/W	0	ADC ALARM Interrupt Enable/Disable. 0 – Interrupts disabled 1 – Interrupts enabled. Note: This is essentially the interrupt mask.

Bit	Identifier	Access	Default	Description
6-4	IRQSEL(2:0)	R/W	000	ADC ALARM Interrupt IRQ Select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11 FYI – same values are other products.
3	ADC_RESET	R/W	0	ADS8668A ADC RESET 0 – deassert reset (normal operation) 1 – assert reset NOTE: Always assert this for >400nsec since the part has some strange modes for shorter resets. Regardless a standard Platform reset will reset the A/D to a power-on reset state.
2	IN_ALARM	RO	N/A	Returns the ADS8668A ADC ALARM status value. 0 – ALARM is deasserted 1 – ALARM is asserted
1	ISTAT_ALARM	RO	N/A	ADC ALARM interrupt status. A read returns the interrupt status. Writing a ‘1’ will clear the interrupt status. This bit is set to a ‘1’ on a transition from low-to-high of the ADC ALARM signal (alarm assertion)
0	IMASK_ALARM	RW	0	ADC ALARM Interrupt Mask: 0 – Interrupt disabled 1 – Interrupt enabled.

DIODIRx (x=1,2) – Digital I/O Direction Control Registers

These two registers control the directions of the 16 digital I/O signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset. If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 16: DIODIR1 – Digital I/O 8-1 Direction Control Register

Bits	Identifier	Access	Default	Description
7-0	DIR_DIO[8:1]	R/W	0x00	Sets the DIOx direction. For each bit: 0 – Input 1 – Output

Table 17: DIODIR2 – Digital I/O 16-9 Direction Control Register

Bits	Identifier	Access	Default	Description
7-0	DIR_DIO[16:9]	R/W	0x00	Sets the DIOx direction. For each bit: 0 – Input 1 – Output

DIOPOLx (x=1,2) – Digital I/O Polarity Control Registers

These two registers control the polarity of the 16 Digital I/O signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset. If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 18: DIOPOL1 – Digital I/O 8-1 Polarity Control Register

Bits	Identifier	Access	Default	Description
7-0	POL_DIO[8:1]	R/W	0x00	Sets the DIOx polarity. For each bit: 0 – No polarity inversion 1 – Invert polarity

Table 19: DIOPOL2 – Digital I/O 16-9 Polarity Control Register

Bits	Identifier	Access	Default	Description
7-0	POL_DIO[16:9]	R/W	0x00	Sets the DIOx polarity. For each bit: 0 – No polarity inversion 1 – Invert polarity

DIOOUTx (x=1,2) – Digital I/O Output Control Registers

These two registers set the DIO output value. This value will only set the actual output if the DIO direction is set as an output. Reading this register does not return the actual input value of the DIO (use the DIOIN register for that). As such, this register can actually be used to detect input/output conflicts.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset. If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 20: DIOOUT1 – Digital I/O 8-1 Output Control Register

Bits	Identifier	Access	Default	Description
7-0	OUT_DIO[8:1]	R/W	0x00	Sets the DIOx output. For each bit: 0 – De-asserts the output (0 if polarity not inverted, 1 if inverted) 1 – Asserts the output (1 if polarity not-inverted, 0 if inverted)

Table 21: DIOOUT2 – Digital I/O 16-9 Output Control Register

Bits	Identifier	Access	Default	Description
7-0	OUT_DIO[16:9]	R/W	0x00	Sets the DIOx output. For each bit: 0 – De-asserts the output (0 if polarity not inverted, 1 if inverted) 1 – Asserts the output (1 if polarity not-inverted, 0 if inverted)

DIOINx (x=1,2) – Digital I/O Input Status Registers

These two registers set the DIO input value. It will read the input value regardless of the setting on the direction (that is, it always reads the input). This reads the actual state of the DIO pin into the part.

Table 22: DIOIN1 – Digital I/O 8-1 Input Status Register

Bits	Identifier	Access	Default	Description
7-0	IN_DIO[8:1]	RO	N/A	Reads the DIO input status. For each bit: 0 – Input de-asserted if polarity not-inverted; asserted if polarity inverted 1 Input asserted if polarity not-inverted; de-asserted if polarity inverted

Table 23: DIOIN2 – Digital I/O 16-9 Input Status Register

Bits	Identifier	Access	Default	Description
7-0	IN_DIO[16:9]	RO	N/A	Reads the DIO input status. For each bit: 0 – Input de-asserted if polarity not-inverted; asserted if polarity inverted 1 Input asserted if polarity not-inverted; de-asserted if polarity inverted

DIOIMASKx (x=1,2) – Digital I/O Interrupt Mask Registers

These two registers are the interrupt mask registers for the digital IOs. The reset type is Platform Reset because interrupts always have to be setup after exiting sleep states.

Table 24: DIOIMASK1 – Digital I/O 8-1 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	IMASK_DIO[8:1]	R/W	0	Digital I/O 8-1 interrupt mask. For each bit: 0 – Interrupt disabled 1 – Interrupt enabled

Table 25: DIOIMASK2 – Digital I/O 16-9 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	IMASK_DIO[16:9]	R/W	0	Digital I/O 16-9 interrupt mask. For each bit: 0 – Interrupt disabled 1 – Interrupt enabled

DIOISTATx (x=1,2) – Digital I/O Interrupt Status Registers

Table 26: DIOISTAT1 – Digital I/O 8-1 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	ISTAT_DIO[8:1]	RW/C	N/A	DIOx interrupt status. A read returns the interrupt status. Writing a ‘1’ clears the interrupt status. This bit is set to a ‘1’ on a transition from low-to-high (POL_DIOx=0) or high-to-low (POL_DIOx=1).

Table 27: DIOISTAT2 – Digital I/O 16-9 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	ISTAT_DIO[16:9]	RW/C	N/A	DIOx interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status. This bit is set to a '1' on a transition from low-to-high (POL_DIOx=0) or high-to-low (POL_DIOx=1).

DIOCR – Digital I/O Control Register

One interrupt can be generated for the 16 digital I/Os. Reset type is Platform.

Table 28: DIOCR – Digital I/O Control Register

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	DIO interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	DIO interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-1	RESERVED	RO	000	Reserved. Writes are ignored; reads always return 0.
0	TMREN	R/W	0	Timer enable signals (used to switch digital I/Os to timer control signals): 0 – Timers disabled 1 – Timers enabled and some DIOs are used based on the TMRFULL setting in the Timer control register (TCR)

AUXDIR – AUX GPIO Direction Control Register

This register controls the direction of the eight AUX GPIO signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset. If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 29: AUXDIR – AUX GPIO Direction Control Register

Bit	Identifier	Access	Default	Description
7-0	DIR_GPIO[8:1]	R/W	0	Sets the direction of the AUX GPIOx lines. For each bit: 0 – Input 1 – Output

AUXPOL – AUX GPIO Polarity Control Register

This register controls the polarity of the eight AUX GPIO signals.

This reset depends on the state of the FPGA_PSEN signal.

- If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset.
- If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 30: AUXPOL – AUX GPIO Polarity Control Register

Bits	Identifier	Access	Default	Description
7-0	POL_GPIO[8:1]	R/W	0	Sets the polarity of the AUX GPIOx lines. For each bit: 0 – No inversion 1 – Invert **Note:** This impacts the polarity as well as the interrupt status edge used.

AUXOUT – AUX GPIO Output Control Register

This register sets the AUX GPIO output value. This value will only set the actual output if the GPIO direction is set as an output. Reading this register does not return the actual input value of the GPIO (use the AUXIN register for that). As such, this register can actually be used to detect input/output conflicts.

This reset depends on the state of the FPGA_PSEN signal.

- If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset.
- If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 31: AUXOUT – AUX GPIO Output Control Register

Bits	Identifier	Access	Default	Description
7-0	OUT_GPIO[8:1]	R/W	0	Sets the AUX GPIOx output values. For each bit: 0 – De-asserts the output (0 if polarity not-inverted, 1 if inverted) 1 – Asserts the output (1 if polarity not-inverted, 0 if inverted)

AUXIN – AUX GPIO I/O Input Status Register

This register sets the AUX GPIO input value. It will read the input value regardless of the setting on the direction (that is, it always reads the input). This reads the actual state of the GPIO pin into the part.

Table 32: AUXIN – AUX GPIO Input Status Register

Bits	Identifier	Access	Default	Description
7-0	IN_GPIOIO[8:1]	RO	N/A	Reads the GPIOx input status. For each bit: 0 – Input de-asserted if polarity not-inverted; asserted if polarity inverted 1 Input asserted if polarity not-inverted; de-asserted if polarity inverted

AUXIMASK – AUX GPIO Interrupt Mask Register

This is the interrupt mask register for the AUX GPIOs and the interrupt enable selection. The reset type is Platform Reset because interrupts always have to be setup after exiting sleep states.

Table 33: AUXICR – AUX GPIO Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	IMASK_GPIO[8:1]	R/W	0	GPIOx interrupt mask. For each bit: 0 – Interrupt disabled 1 – Interrupt enabled

AUXISTAT – AUX GPIO I/O Interrupt Status Register

Table 34: AUXISTAT – AUX GPIO Interrupt Status Register

Bits	Identifier	Access	Default	Description
7-0	ISTAT_GPIO[8:1]	RW/C	N/A	GPIOx interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status. This bit is set to a '1' on a transition from low-to-high (POL_DIOx=0) or high-to-low (POL_DIOx=1).

AUXMODE1– AUX I/O Mode Register #1

These two registers select the mode on each AUX GPIO.

This reset depends on the state of the FPGA_PSEN signal.

- If FPGA_PSEN is a ‘0’ then the reset is the power-on and Platform Reset.
- If FPGA_PSEN is a ‘1’ then this register is only reset at power-on.

Table 35: AUXMODE1 – AUX I/O Mode Register

Bit	Identifier	Access	Default	Description
7	MODE_GPIO8	R/W	0	GPIO8 mode. 0 – GPIO (I/O) 1 – ICTC3 (input)
6	MODE_GPIO7	R/W	0	GPIO7 mode. 0 – GPIO (I/O) 1 – ICTC4 (input)
5	MODE_GPIO6	R/W	0	GPIO6 mode. 0 – GPIO (I/O) 1 – OCTC3 (output)
4	MODE_GPIO5	R/W	0	GPIO5 mode. 0 – GPIO (I/O) 1 – OCTC4 (output)
3	MODE_GPIO4	R/W	0	GPIO4 mode. 0 – GPIO (I/O) 1 – WDOG_RESET# (output only). In this mode, the GPIO will be the FPGA watchdog timer trigger output that signals external equipment that the watchdog fired. The GPIO input status can still be read. Default is low-true. Setting GPIO polarity to ‘1’ makes it high-true.
2	MODE_GPIO3	R/W	0	GPIO3 mode. 0 – GPIO (I/O) 1 – WAKE# (input only). In this mode, the GPIO is passed through to the PCI_WAKE# signal. Default is low-true. Setting GPIO polarity to ‘1’ makes it high-true. The GPIO input status can still be read.
1	MODE_GPIO2	R/W	0	GPIO2 mode. 0 – GPIO (I/O) 1 – W_DISABLE# (input only). In this mode, the GPIO is passed through to the W_DISABLE# signal. The GPIO input status can still be read. Default is low-true. Setting GPIO polarity to ‘1’ makes it high-true.
0	MODE_GPIO1	R/W	0	GPIO1 mode. 0 – GPIO (I/O) 1 – SLEEP# (input only). This is the sleep signal on the baseboard power connector. It passes through the SLEEP# input on the CPU module. Default is low-true. Setting GPIO polarity to ‘1’ makes it high-true.

WDT_CTL – Watchdog Control Register

Reset type is Platform.

Table 36: WDT_CTL – Watchdog Control Register

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	Watchdog interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	Watchdog interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
2	RESET_EN	R/W	0	Enable the Watchdog to assert the push-button reset if it "fires". 0 – Watchdog will not reset the board 1 – Board will be reset if the Watchdog "fires"
1	WDT_EN	R/W	0	Watchdog Enable: 0 – Watchdog is disabled 1 – Watchdog is enabled **Note:** The WDT_VAL register must be set before enabling.
0	WDT_STAT	RO	0	Watchdog Status: 0 – Watchdog disabled or watchdog has not "fired" 1 – Watchdog fired. **Note:** Once set to a '1', it will remain so until any of the following occurs: • the WDT_VAL register is written to • the WDT_EN is disabled • a reset occurs

WDT_VAL – Watchdog Value Register

This register sets the number of seconds for a Watchdog prior to enabling the watchdog. By writing this value, the watchdog can be prevented from "firing". A watchdog fires whenever this registers value is all 0s, so it must be set to a non-zero value before enabling the watchdog to prevent an immediate "firing".

Reset type is Platform.

The value written should always be 1 greater than the desired timeout value due to a 0-1 second "tick" error band (values written should range from 2-255 because a 1 could cause an immediate trigger); that is, the actual timeout is WDT_VAL seconds with a -1 second to 0 second error band.

Table 37: WDT_VAL – Watchdog Control Register

Bits	Identifier	Access	Default	Description
7-0	WDT_VAL(7:0)	R/W	0x00	Number of seconds before the Watchdog fires. By default, it is set to zero which results in an immediate watchdog if WDT_EN is set to a '1'.

XCVRMODE – COM Transceiver Mode Register

Sets the RS232 vs RS422/485 mode on the COM port transceivers. These drive the UART_SEL signals from the FPGA to the transceivers.

Reset type is Platform.

Table 38: XCVRMODE – COM Transceiver Mode Register

Bits	Identifier	Access	Default	Description
7-4	Reserved	RO	0000	Reserved. Writes are ignored; reads always return 0.
3-2	Reserved	RO	00	Reserved. Writes are ignored; reads always return 0.
3	COM4_MODE	R/W	0	COM4 Transceiver mode: 0 – RS232 1 – RS422/485
2	COM3_MODE	R/W	0	COM3 Transceiver mode: 0 – RS232 1 – RS422/485
1	COM2_MODE	R/W	0	COM2 Transceiver mode: 0 – RS232 1 – RS422/485
0	COM1_MODE	R/W	0	COM1 Transceiver mode: 0 – RS232 1 – RS422/485

AUXMODE2– AUX I/O Mode Register #2

This register defines the interrupt mapping for the AUX GPIOs.

Reset type is Platform.

Table 39: AUXMODE2 - AUX I/O Mode Register #2

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	AUX GPIO interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	AUX GPIO interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	Reserved	RO	0000	Reserved. Writes are ignored; reads always return 0.

FANCON – Fan Control Register

The fan is always off in any sleep mode. When the processor comes out of sleep this register must be setup again since it will be reset to default by the platform reset signal. The fan is always turned “off” in sleep modes.

On other products the FPGA controlled the fan and monitored fan speed. The FPGA on this products does that as well but the COM Module can also control the fan (either on/off or PWM) and monitor the fan speed. The FPGA currently only allows the fan to be turned on or off (no PWM since that requires interleaved fan-speed monitoring). This is the same case with the COM Module unless a 4-wire fan is used in which case the COM Module can use PWM fan-speed control and monitor fan speed.

On all FPGA releases after DEV-0.02 (which only support the R1B PCB rev 0.20A or later) the fan tach signal is monitored by both the FPGA and COM Module all the time (COM_MODE does not impact this). The only purpose of COM_MODE is to select whether the COM Module or the FPGA controls the fan on/off (or PWM speed should that be used on the COM Module).

Reset type is Reset.

Table 40: FANCON – Fan Control Register

Bits	Identifier	Access	Default	Description
7	COM_MODE	R/W	1	Selects the COM Module fan control instead of the FPGA. 0 – FPGA controls fan on/off. 1 – COM Module controls fan on/off (or PWM if used) . **Note:** COM Module will only operate with 4-wire fans if using PWM speed control. 3-wire fans are fine as long as it is just turned on or off. PWM speed can be used with either type fan but the fan-tach readings will not be stable on a 3-wire fan (but could possibly still be used to monitor if the fan is stuck or not).
6-1	RESERVED	RO	0	Reserved – Writes are ignored. Reads always return 0
0	FAN_OFF	R/W	0	Fan Disable: 0 – Fan is On 1 – Fan is Off **Note**: On is the default in case there is no software turning it on. This control only applies when COM_MODE is a '0' (FPGA controls fan on/off).

FANTACHLS, FANTACHMS – FANTACH STATUS REGISTERS

The FPGA fan tach readings are always available and do not depend on either COM_MODE or the FAN_OFF settings.

The number of fan tach output samples over a 1 second sampling period. The value is always valid after the fan speed stabilizes and is updated every 1 sec (after a delay of 1 sec). Currently only the lower 10-bits have a valid tach reading (i.e., the upper 6 bits will always be zero). The fan tach count should never overflow in the 1 second period but it if does the value will "stick" at 0x03FF.

The design can handle up at least a 10,000 rpm fan with a fan tach output of up to 4 uniform pulses per revolution. The duty cycle of the fan tach output pulse can be as low as 25% (typically they are very close to 50%). The conversion to RPM is:

RPM = (FANTACH x 60) / PPR

Where,

FANTACH - the 16-bit register reading
PPR – fan tach pulses per revolution (typ either 1,2 or 4)

Reset type: Not Applicable

Table 41: FANTACHLS – FANTACH Status Register LS Bits

Bits	Identifier	Access	Default	Description
7-0	FANTACH[7:0]	RO	N/A	LS 8-bits of FANTACH (read this first since it latches the value for the MS 8 bits)

Table 42: FANTACHMS – FANTACH Status Register MS Bits

Bits	Identifier	Access	Default	Description
7-0	FANTACH[15:8]	RO	N/A	LS 8-bits of FANTACH (read this first since it latches the value for the MS 8 bits)

Note: The FANTACHLS register must be read first. It will latch a copy of the MS bits so that when FANTACHMS is read it is based on the same 16-bit value. This assumes that a 16-bit word read on the LPC bus read the even (LS) address before the odd (MS) address.

UART1CR – UART1 Control Register (COM1)

Reset type is Platform.

Note: The BIOS (via ACPI) may modify this register when in an ACPI-capable operating system. The register can be read for status purposes but do not write to it unless you are using a non-ACPI operating system.

Table 43: UART1CR – UART1 Control Register (COM1)

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	UART interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	001	UART interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 **[← COM1 Default]** 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	UART1_BASE(3:0)	R/W	0000	UART Base Address: 0000 - 3F8h **[← COM1 Default]** 0001 - 2F8h 0010 - 3E8h 0011 - 2E8h 0100 - 200h 0101 - 220h 0110 - 228h 0111 - 338h 1000 - 238h 1001 - 338h 1010-1111 **[← These values are reserved; do not use.]**

UART2CR – UART2 Control Register (COM2)

Reset type is Platform.

Table 44: UART2CR – UART2 Control Register (COM2)

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	UART interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	UART interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 **[← COM2 Default]** 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	UART2_BASE(3:0)	R/W	0001	UART Base Address: 0000 - 3F8h 0001 - 2F8h **[← COM2 Default]** 0010 - 3E8h 0011 - 2E8h 0100 - 200h 0101 - 208h 0110 - 220h 0111 - 228h 1000 - 238h 1001 - 338h 1010-1111 **[← These values are reserved; do not use.]**

UART3CR – UART3 Control Register (COM3)

Reset type is Platform.

Table 45: UART3CR – UART3 Control Register (COM3)

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	UART interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	101	UART interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7**[← COM3 Default]** 110 – IRQ9 111 – IRQ11
3-0	UART2_BASE(3:0)	R/W	0010	UART Base Address: 0000 - 3F8h 0001 - 2F8h 0010 - 3E8h **[← COM3 Default]** 0011 - 2E8h 0100 - 200h 0101 - 208h 0110 - 220h 0111 - 228h 1000 - 238h 1001 - 338h 1010-1111 **[← These values are reserved; do not use.]**

UART4CR – UART4 Control Register (COM4)

Reset type is Platform.

Table 46: UART4CR – UART4 Control Register (COM4)

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	UART interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	011	UART interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10**[← COM4 Default]** 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	UART2_BASE(3:0)	R/W	0011	UART Base Address: 0000 - 3F8h 0001 - 2F8h 0010 - 3E8h 0011 - 2E8h **[← COM4 Default]** 0100 - 200h 0101 - 208h 0110 - 220h 0111 - 228h 1000 - 238h 1001 - 338h 1010-1111 **[← These values are reserved; do not use.]**

UARTMODE1 – UART MODE REGISTER #1

When the COM Transceiver Mode is set to RS422/485 (in the **XCVRMODE** register) and the RS-485 Automatic Direction Control is enabled (e.g., **UART1_485ADC** set to ‘1’) then the transceiver Tx output is enabled. When there are bytes to transmit and the transceiver Tx output is disabled (i.e., tri-stated) when there are no bytes to transmit.

When the COM Transceiver Mode is set to RS422/485 and Automatic Direction Control is disabled (e.g., **UART1_485ADC** set to ‘0’) then the UART is in Manual Direction Control mode and the transceiver Tx output enable is controlled by software using the **RTS** bit in the UART Modem Control Register.

RTS = '0' **-** Transceiver Tx output is enabled.

RTS = '1' **-** Transceiver Tx output is disabled (i.e., tri-stated).

Warning: Terminal software, expecting an RS-232 port, may set **RTS** to '1' and disable the transmitter when initializing an RS-422/485 port in Manual Direction Control mode. Application software that handles the RS-422/485 port should set **RTS** to '0' to enable transmitting when in Manual Direction Control mode.

Reset type is Platform.

Table 47: UARTMODE1 – UART MODE Register #1

Bits	Identifier	Access	Default	Description
7	UART4_485ADC	R/W	0	COM4 RS-485 Automatic Direction Control: 0 – Disabled 1 – Enabled **Note:** Only enable in RS-485 mode. The COM4_MODE in XCVRMODE register must also be set to a '1'
6	UART3_485ADC	R/W	0	COM3 RS-485 Automatic Direction Control: 0 – Disabled 1 – Enabled **Note:** Only enable in RS-485 mode. The COM3_MODE in XCVRMODE register must also be set to a '1'
5	UART2_485ADC	R/W	0	COM2 RS-485 Automatic Direction Control: 0 – Disabled 1 – Enabled **Note:** Only enable in RS-485 mode. The COM2_MODE in XCVRMODE register must also be set to a '1'
4	UART1_485ADC	R/W	0	COM1 RS-485 Automatic Direction Control: 0 – Disabled 1 – Enabled **Note:** Only enable in RS-485 mode. . The COM1_MODE in XCVRMODE register must also be set to a '1'
3	UART4_EN	R/W	0	UART #4 Output Enable: 0 – Tx and RTS outputs are disabled 1 – Tx and RTS outputs are enabled Note: If disabled the UART I/O space is freed up.
2	UART3_EN	R/W	0	UART #3 Output Enable: 0 – Tx and RTS outputs are disabled 1 – Tx and RTS outputs are enabled **Note:** If disabled the UART I/O space is freed up.
1	UART2_EN	R/W	0	UART #2 Output Enable: 0 – Tx and RTS outputs are disabled 1 – Tx and RTS outputs are enabled **Note:** If disabled the UART I/O space is freed up.
0	UART1_EN	R/W	0	UART #1 Output Enable: 0 – Tx and RTS outputs are disabled 1 – Tx and RTS outputs are enabled **Note:** If disabled the UART I/O space is freed up.

UARTMODE2 – UART MODE REGISTER #2

Standard software (the BIOS and the operating system) assumes the baud-rate clock is 1.8432 MHz and programs the divisors accordingly; however, a faster oscillator is needed for baud rates higher than 115,200.

The FAST_MODE bit in this register shifts the divisor by 4 bits (multiply by 16) so that the legacy baud rate comes out correctly for the 16x UART clock. This bit must be set to use rates above 115,200 and may require custom software.

Reset type is Platform.

Note: The values shown are for the default BIOS configuration.

Table 48: UARTMODE2 – UART MODE Register #2

Bits	Identifier	Access	Default	Description
7-1	Reserved	RO	0000000	Reserved. Writes are ignored; reads always return 0.
0	FAST_MODE	R/W	0	Sets how the baud-rate divisor for the 16550 UARTs are interpreted (applies to all ports): 0 – Divisor is multiplied by 16 (legacy mode for 1.8432 MHz clock) 1 – Divisor is not modified (fast mode for 16x 1.8432 MHz clock) **Note:** This must be set to ‘1’ to use baud rates above 115,200.

Programming Information for Hardware Interfaces

4

Watchdog Timer

A Watchdog timer is implemented within the FPGA. When triggered, the Watchdog timer can set a status bit, generate an interrupt and/or hit the push-button-reset. The Watchdog timer implements a 1-255 second timeout.

The Watchdog time out is set in an 8-bit register (WDT_VAL). When the Watchdog is enabled, the WDT_VAL will start to count down. If the Watchdog is enabled and whenever WDT_VAL is zero, the Watchdog is triggered (so a non-zero value must be written before enabling the watchdog). Software must periodically write a non-zero value to WDT_VAL to prevent this trigger. The value written should always be 1 greater than the desired timeout value due to a 0-1 second error band. Values written should be from 2-255 because a 1 could cause an immediate trigger); that is, the actual timeout is WDT_VAL seconds with a -1 second to 0 second error band.

The Watchdog control/status register(s) have bits for the following:

- Watchdog enable/disable (disabled by default)
- Watchdog timeout status (This is cleared when the Watchdog is disabled or when a new value is written to WDT_VAL. Writing WDT_VAL would be the interrupt-acknowledge.)
- Watchdog interrupt IRQ select (from the same list of eight interrupts supported on the LPC SERIRQ)
- Interrupt enable
- Board reset enable (when set, the board will be reset when the Watchdog timer expires).

Programmable LED

User I/O connector J2 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J2, pin 16; connect the anode to +3.3 V. An on-board resistor limits the current when the circuit is turned on. A programmable LED is provided on the CBR-4005B paddleboard. Refer to the *VL-EPU-4562 Hardware Reference Manual* for the location of the Programmable LED on the CBR-4005B paddleboard.

To switch the PLED on and off, refer to Table 3: PCR – Product Code and LED Register, on page 8.

Processor WAKE# Capabilities

The following devices can wake up the processor using the PCIE_WAKE# signal to the CPU module:

- I210 Ethernet controller
- Minicard #1 WAKE# signal
- Minicard #2 WAKE# signal
- FPGA via a secondary function on one of the 8x GPIOs

The following USB devices can wake up the processor using the in-band SUSPEND protocol:

- On-board USB 3.0 port
- Any of the four USB Ports on the CBR-4005B paddleboard
- Minicard #1 USB port
- Minicard #2 USB port

*** *End of document* ***