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Evaluation Board for the ADuM7223 *i*Coupler, 4 A, Isolated Precision Half Bridge Driver

FEATURES

4 A peak output current
High frequency operation: 1 MHz maximum
CMOS input logic levels
4.5 V to 18 V output drive
Supports TO-252 IGBT/MOSFETs
Bootstrap option

SUPPORTED *i*Coupler MODELS

ADuM7223A
ADuM7223B
ADuM7223C

GENERAL DESCRIPTION

The EVAL-ADuM7223EBZ supports the ADuM7223 4 A, isolated precision half bridge driver. Because the evaluation boards have footprints for insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs) in TO-252 packages, the ADuM7223 can be evaluated with many different power devices. The evaluation boards also allow the high-side supply to be bootstrapped to the low-side supply.

The ADuM7223A model represents a superset of the ADuM7223 models because it has the lowest minimum output voltage (4.5 V). The evaluation board comes populated with the lowest undervoltage lockout (UVLO) value (Grade A).

Complete information about the ADuM7223 is available in the ADuM7223 data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD DIAGRAM

Figure 1. ADuM7223 Evaluation Board

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REVISION HISTORY

3/14—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

PAD LAYOUT FOR THE DEVICE UNDER TEST (DUT)

Figure 5 shows the top layer artwork for the dual gate driver circuit.

- U1 is the footprint for the ADuM7223.
- C1, C2, and C4 are 0.1 µF bypass capacitors; C3 and C5 are 10 µF bypass capacitors.
- Q1 and Q2 can be populated with TO-252 MOSFETs or IGBTs with the pinout shown in Figure 2.
- C6 and C7 are 2.2 nF loads for the gate driver outputs. Remove C6 and C7 if MOSFETs or IGBTs are added to Q1 and Q2.
- R6 and R7 are gate resistors that control the edges of the outputs. By default, 0 Ω resistors are installed; however, these resistors may need to be replaced with low value 0603 resistors if the outputs have loads lighter than 2.2 nF.

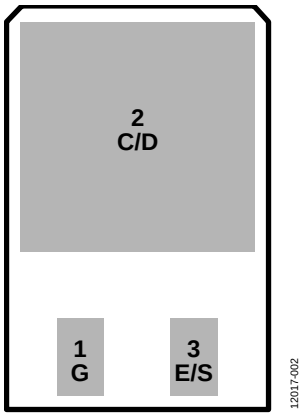

Figure 2. IGBT/MOSFET Footprint

POWER CONNECTIONS

To connect the evaluation board to the power supply, follow these steps:

1. Connect the 5 V or 3.3 V input supply to JP2 with the positive terminal on VDD1 and the ground on GND1.
2. Connect the ADuM7223 V_{DDB} supply voltage (4.5 V to 18 V) to the VDDB pin and its return to the GNDB pin.
3. Connect the VDDA supply voltage (4.5 V to 18 V) to the pin marked VDDA and its return to GNDA.

GNDA and GNDB are functionally isolated. The emitter/source of Q1 is tied to GNDA, and the emitter/source of Q2 is tied to GNDB. GNDB also has a wire pad directly below the emitter/source pad of Q2. Connect the bridge supply to the +HV wire pin, which is connected to the collector/drain of Q1 if Q1 and Q2 are populated.

INPUT/OUTPUT CONNECTIONS

Connect Logic Input A (V_{IA}) to VIA or to Pin 1 of J1; connect Logic Input B (V_{IB}) to VIB or to Pin 2 of J1. Both inputs have 50 Ω terminations. Resistor R5 enables the outputs of the ADuM7223 by pulling the DISABLE pin low. The disable function can also be externally controlled from J1 or set by J2 using a 2-pin jumper.

The half bridge output is the Q1 emitter/source and Q2 collector/drain node. VOUT is the output of the half bridge, and it is also connected to GNDA.

BOOTSTRAPPING VDDB TO VDDA

To bootstrap VDDB to VDDA, D1 can be populated with a diode from VDDB to VDDA, as shown in Figure 3. Additionally, populate R8 with a value between 0 Ω and 10 Ω to control the charge rate of the C2 and C3 bootstrap capacitors. In this way, both outputs of the ADuM7223 can be powered by the VDDB supply when a half bridge is configured with Q1 and Q2. Additional overvoltage protection can be added by populating D2 with a zener diode if desired.

When the switch node (GNDA) is low, C2 and C3 are charged through the forward-biased bootstrapping diode. When the switch node rises to the bridge voltage, the diode becomes reverse biased, and VDDA = GNDA + VDDB − GNDB because of the charge on C2 and C3. For bootstrapping to work, Q1 and Q2 must be populated instead of the load capacitors, C6 and C7. The switching frequency and duty cycle must be sufficiently high to supply C2 and C3 with the charge required to drive the Q1 gate.

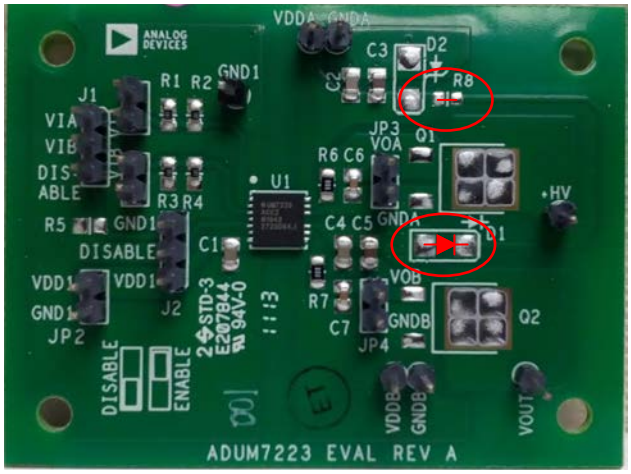

Figure 3. Bootstrapping VDDB to VDDA

EVALUATION BOARD SCHEMATIC

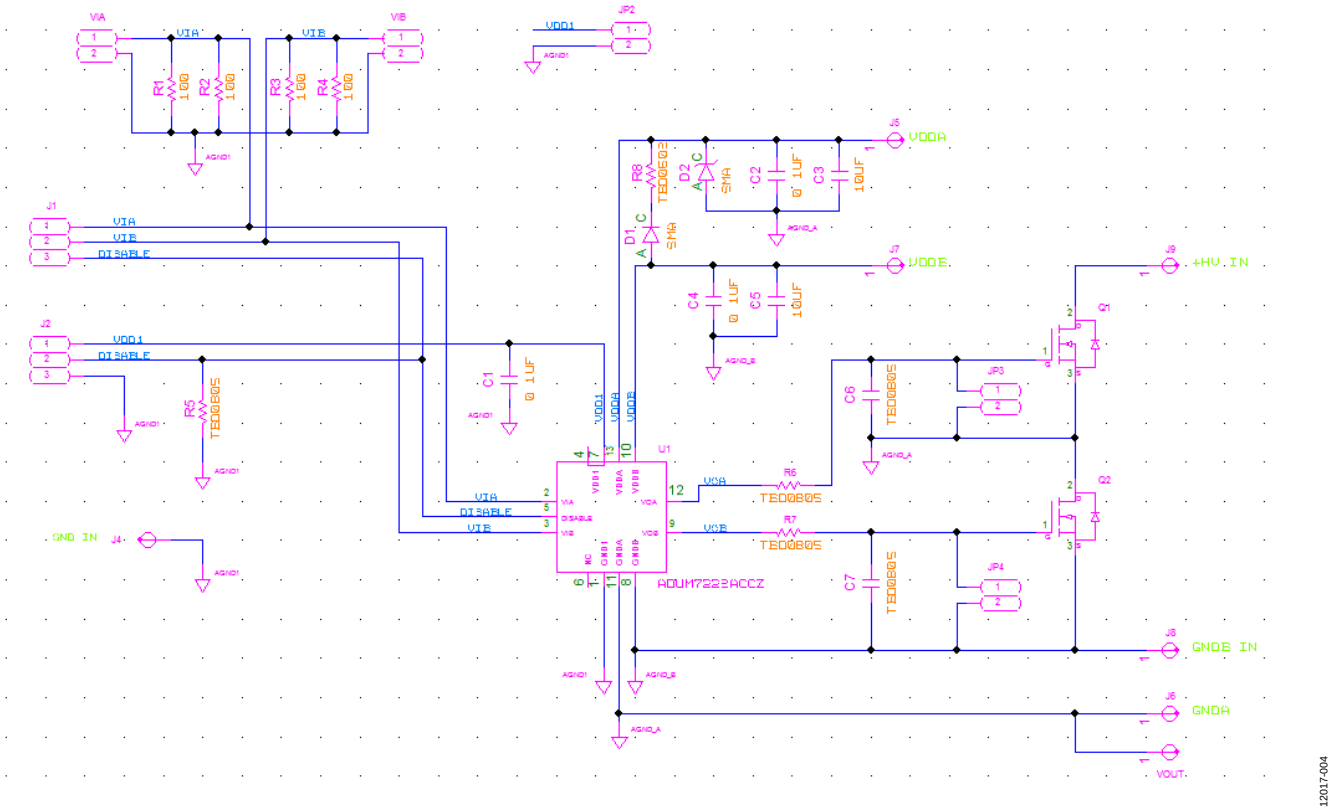

Figure 4. Half Bridge Driver Schematic

EVALUATION BOARD LAYOUT

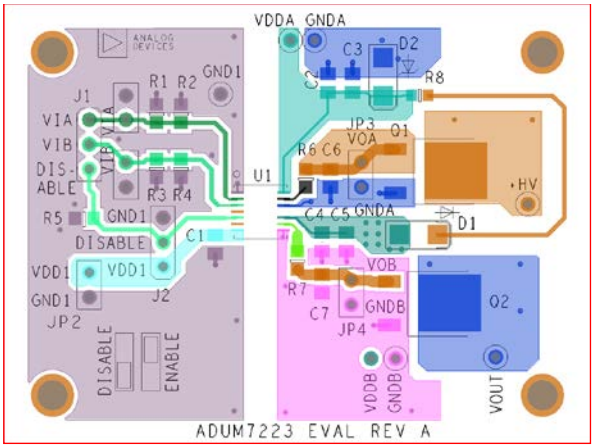

Figure 5. ADuM7223 Evaluation Board Top Layer

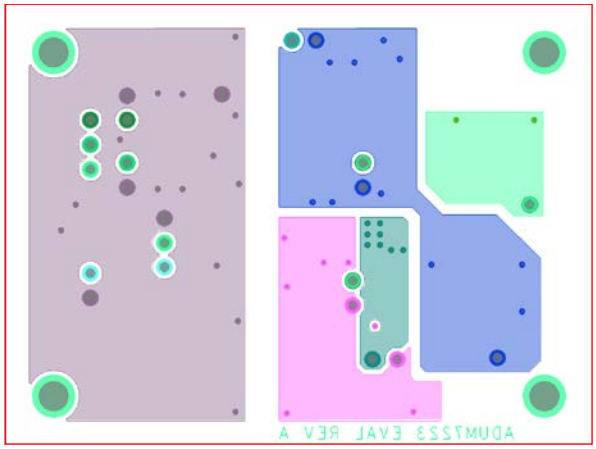

Figure 6. ADuM7223 Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description
1	U1	ADuM7223ACCZ IC
3	C1, C2, C4	Capacitor, 0.1 µF, 25 V, 10%, 0603
2	C3, C5	Capacitor, 10 µF, 25 V, 10%, 1206
2	C6, C7	Capacitor, 2200 pF, 50 V, 5%, 0603
3	J3, J5, J7	Test point, TP-104 series, red
3	J4, J6, J8	Test point, TP-104 series, black
4	R1, R2, R3, R4	Resistor, 100 Ω, 1/4 W, 1%, 0805
1	R5	Resistor, 10 kΩ, 1/4 W, 1%, 0805
2	R6, R7	Resistor, 0 Ω, 1/10 W, 0603
4	TP1, TP2, TP3, TP4	Test point, TP-104 series, white
4	J1, J2, Q1, Q2	Not installed

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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